

**U.S. UTILITY Patent Application**

## O.I.P.E.

**PATENT DATE**

APPLICATION NO.  
09/883990

CONT/PRIOR  
F

CLASS 438 *326*

SUBCLASS

ART UNIT

**EXAMINER**

Eiji Koyama

327

342

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2. 0/2

Vileica

Conductor Integrated Circuit

## ISSUING CLASSIFICATION

[illegible]

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	<div style="border-bottom: 1px solid black; margin-bottom: 5px;"> <span style="float: left;">(Assistant Examiner)</span> <span style="float: right;">(Date)</span> </div> <div style="border-bottom: 1px solid black; margin-bottom: 5px;"> <span style="float: left;">(Primary Examiner)</span> <span style="float: right;">(Date)</span> </div> <div style="border-bottom: 1px solid black; margin-bottom: 5px;"> <span style="float: left;">(Legal Instruments Examiner)</span> <span style="float: right;">(Date)</span> </div>			<b>NOTICE OF ALLOWANCE MAILED</b>	
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				Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.				<b>ISSUE BATCH NUMBER</b>	
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